CLAIMS:

1. A method of forming a capacitor comprising:

forming a capacitor storage node having an uppermost surface and an overlying insulative material over the uppermost surface;

after forming the capacitor storage node and the overlying insulative material, forming a capacitor dielectric functioning region discrete from the overlying insulative material operably proximate at least a portion of the capacitor storage node; and

forming a cell electrode layer over the capacitor dielectric functioning region and the overlying insulative material.

2. The method of claim 1, wherein the forming of the capacitor storage node comprises:

forming a layer of material over a substrate;

forming an opening received within the layer of material; and

forming a layer of conductive material within the opening to less than fill the opening.

3. The method of claim 1, wherein the forming of the capacitor storage node comprises:

forming a layer of material over a substrate;

forming an opening received within the layer of material;

overfilling the opening with conductive material; and

removing a sufficient amount of the conductive material to less than fill the opening.

4. The method of claim 1, wherein the forming of the capacitor storage node comprises:

forming a layer of material over a substrate, the layer of material having a generally planar outer surface; and

forming the storage node to be received within the layer of material and to have an upper surface elevationally below the generally planar outer surface.

5. The method of claim 1, wherein:

the forming of the capacitor storage node comprises:

forming a layer of material over a substrate;

forming an opening received within the layer of material; and

forming a layer of conductive material within the opening to less than fill the opening; and

the forming of the insulative material comprises filling remaining opening portions with the insulative material.

6. The method of claim 1, wherein:

the forming of the capacitor storage node comprises:

forming a layer of material over a substrate, the layer of material having a generally planar outer surface;

forming the storage node to be received within the layer of material and to have an upper surface elevationally below the generally planar outer surface; and

the forming of the insulative material comprises forming a sufficient amount of the insulative material over the storage node to have an insulative material surface which is generally coplanar with the generally planar outer surface of the layer of material.

7. The method of claim 1, wherein:

the forming of the capacitor storage node comprises:

forming a layer of material over a substrate;

forming an opening received within the layer of material; and

forming a layer of conductive material within the opening to less than fill the opening; and

prior to the forming of the capacitor dielectric function region, etching the layer of material selectively relative to the insulative material and exposing a side surface of the storage node.

8. The method of claim 7 further comprising forming a layer of roughened polysilicon over the exposed side surface of the storage node.

9. The method of claim 1 further comprising after the forming of the cell electrode layer, conducting a maskless etch of the cell electrode layer leaving cell electrode material only over generally vertical surfaces.

10. The method of claim 1, wherein the forming of the capacitor storage node comprises forming said node as a capacitor storage node container.

11. A method of forming a capacitor comprising:

forming a capacitor storage node having an uppermost surface and a side surface joined therewith;

forming a protective cap over the uppermost surface;

forming a capacitor dielectric layer over the side surface and protective cap; and

forming a cell electrode layer over the side surface of the capacitor storage node.

12. The method of claim 11, wherein the forming of the capacitor storage node comprises:

forming a layer of material over a substrate;

forming an opening received within the layer of material; and

forming conductive material within the opening.

13. The method of claim 11, wherein the forming of the capacitor storage node comprises:

forming a layer of material over a substrate;

forming an opening received within the layer of material; and

filling the opening with conductive material.

14. The method of claim 11, wherein:

the forming of the capacitor storage node comprises:

forming a layer of material over a substrate;

forming an opening received within the layer of material; and

less than filling the opening with conductive material; and

the forming of the protective cap comprises forming the cap at least within a remaining opening portion.

15. The method of claim 11, wherein the forming of the capacitor storage node comprises forming conductive material laterally adjacent a layer of material, and further comprising after the forming of the protective cap, removing material of the laterally adjacent layer of material and exposing a side surface portion of the storage node.

16. The method of claim 11, wherein the forming of the capacitor storage node comprises forming conductive material laterally adjacent a layer of material, and further comprising after the forming of the protective cap, selectively etching material of the laterally adjacent layer of material relative to the protective cap and exposing a side surface portion of the storage node.

17. The method of claim 11, wherein the forming of the cell electrode layer comprises forming the cell electrode layer over the protective cap and storage node side surface, and removing material of the cell electrode layer from over protective cap.

18. The method of claim 11, wherein the forming of the cell electrode layer comprises forming the cell electrode layer over the protective cap and storage node side surface, and without a mask, anisotropically etching the cell electrode layer.

19. The method of claim 11, wherein:

the forming of the capacitor storage node comprises forming conductive material laterally adjacent a layer of material, and further comprising after the forming of the protective cap, removing material of the laterally adjacent layer of material and exposing a side surface portion of the storage node; and

the forming of the cell electrode layer comprises forming the cell electrode layer over the protective cap and the storage node side surface portion which was exposed, and anisotropically etching the cell electrode layer.

20. The method of claim 11, wherein:

the forming of the capacitor storage node comprises forming conductive material laterally adjacent a layer of material, and further comprising after the forming of the protective cap, selectively etching material of the laterally adjacent layer of material relative to the protective cap and exposing a side surface portion of the storage node; and

the forming of the cell electrode layer comprises forming the cell electrode layer over the protective cap and the storage node side surface portion which was exposed, and anisotropically etching the cell electrode layer.

21. The method of claim 11, wherein the forming of the protective cap comprises forming said cap from insulative material.

22. A method of forming a plurality of capacitors comprising:

forming a plurality of capacitor storage nodes arranged in columns;

forming a capacitor dielectric layer over at least portions of the capacitor storage nodes;

forming a common cell electrode layer over the plurality of capacitor storage nodes;

removing cell electrode layer material from between the columns and isolating individual cell electrodes over individual respective capacitor storage nodes; and

after the removing of the cell electrode layer material, forming conductive material over portions of remaining cell electrode material and placing some of the individual cell electrodes into electrical communication with one another.

23. The method of claim 22, wherein the forming of the capacitor storage nodes comprises:

forming an insulative layer of material;

forming openings received within the insulative layer of material; and

forming conductive material received within the openings.

24. The method of claim 22, wherein the forming of the capacitor storage nodes comprises:

forming an insulative layer of material;

forming openings received within the insulative layer of material;

overfilling the openings with conductive material; and

removing portions of the conductive material and isolating the capacitor storage nodes within the openings.

25. The method of claim 22, wherein the forming of the capacitor storage nodes comprises:

forming a first insulative layer of material;

forming openings received within the first insulative layer of material;

overfilling the openings with conductive material;

removing portions of the conductive material to below an outer surface of the first insulative layer of material;

forming a second different insulative layer of material at least within remaining opening portions; and

removing material of the first insulative layer of material selectively relative to material of the second insulative layer of material and exposing a side surface of the conductive material.

26. The method of claim 22, wherein the removing of the cell electrode layer material comprises anisotropically etching the cell electrode layer material.

27. The method of claim 22, wherein the forming of the conductive material over the remaining cell electrode material portions comprises:

forming an insulative layer of material over the remaining cell electrode material;

exposing at least some of the remaining cell electrode material portions through the insulative layer; and

forming the conductive material over the remaining cell electrode material portions.

28. The method of claim 22, wherein the forming of the conductive material over the remaining cell electrode material portions comprises:

forming an insulative layer of material over the remaining cell electrode material;

etching a trench into the insulative layer and exposing at least some of the remaining cell electrode material portions; and

forming the conductive material within the trench.

29. The method of claim 22, wherein the forming of the conductive material over the remaining cell electrode material portions comprises:

forming an insulative layer of material over the remaining cell electrode material;

etching a trench into the insulative layer and exposing at least some of the remaining cell electrode material portions;

forming the conductive material within the trench; and

planarizing the conductive material within the trench relative to an insulative layer outer surface.

30. The method of claim 22, wherein:

the forming of the capacitor storage nodes comprises:

forming a first insulative layer of material;

forming openings received within the first insulative layer of material;

overfilling the openings with conductive material;

removing portions of the conductive material to below an outer surface of the first insulative layer of material;

forming a second different insulative layer of material at least within remaining opening portions; and

removing material of the first insulative layer of material selectively relative to material of the second insulative layer of material and exposing a side surface of the conductive material; and

the removing of the cell electrode layer material comprises anisotropically etching the cell electrode layer material.

31. The method of claim 22, wherein:

the forming of the capacitor storage nodes comprises:

forming a first insulative layer of material;

forming openings received within the first insulative layer of material;

overfilling the openings with conductive material;

removing portions of the conductive material to below an outer surface of the first insulative layer of material;

forming a second different insulative layer of material at least within remaining opening portions; and

removing material of the first insulative layer of material selectively relative to material of the second insulative layer of material and exposing a side surface of the conductive material; and

the forming of the conductive material over the remaining cell electrode material portions comprises:

forming a third insulative layer of material over the remaining cell electrode material;

exposing at least some of the remaining cell electrode material portions through the third insulative layer; and

forming the conductive material over the remaining cell electrode material portions.

32. The method of claim 22, wherein:

the forming of the capacitor storage nodes comprises:

forming a first insulative layer of material;

forming openings received within the first insulative layer of material;

overfilling the openings with conductive material;

removing portions of the conductive material to below an outer surface of the first insulative layer of material;

forming a second different insulative layer of material at least within remaining opening portions; and

removing material of the first insulative layer of material selectively relative to material of the second insulative layer of material and exposing a side surface of the conductive material; and

the forming of the conductive material over the remaining cell electrode material portions comprises:

forming a third insulative layer of material over the remaining cell electrode material;

etching a trench into the third insulative layer and exposing at least some of the remaining cell electrode material portions; and

forming the conductive material within the trench.

33. A method of forming a plurality of capacitors comprising:

forming a plurality of capacitor storage nodes having respective capacitor dielectric layers disposed thereover, the capacitor storage nodes being arranged in columns;

forming a common cell electrode layer over the plurality of capacitor storage nodes;

without masking, etching the common cell electrode layer to electrically isolate individual cell electrodes over individual respective capacitor storage nodes; and

electrically interconnecting selected electrically isolated individual cell electrodes.

34. The method of claim 33, wherein:

the forming of the capacitor storage nodes comprises forming respective storage node upper surfaces and side surfaces joined therewith, the respective side surfaces having first portions which are disposed elevationally higher than an adjacent insulative material upper surface, and second portions which are disposed elevationally lower than the adjacent insulative material upper surface; and

the forming of the common cell electrode layer comprises forming the layer laterally proximate the respective side surface first portions.

35. The method of claim 33 further comprising prior to the forming of the common cell electrode layer, forming individual insulative material caps over the capacitor storage nodes.

36. The method of claim 33, wherein:

the forming of the capacitor storage nodes comprises forming respective storage node upper surfaces and side surfaces joined therewith, the respective side surfaces having first portions which are disposed elevationally higher than an adjacent insulative material upper surface, and second portions which are disposed elevationally lower than the adjacent insulative material upper surface; and

after the forming of the capacitor storage nodes, forming individual insulative material caps over the capacitor storage nodes' upper surfaces, and wherein the forming of the common cell electrode layer comprises forming the layer laterally proximate the respective side surface first portions.

37. The method of claim 33, wherein:

the forming of the plurality of capacitor storage nodes comprises:

forming an insulative layer;

forming individual storage nodes received within the insulative layer; and

removing material of the insulative layer and partially exposing respective storage node portions; and

the etching of the common cell electrode layer comprises forming individual cell electrode bands around the node portions which were previously exposed.

38. The method of claim 33, wherein:

the forming of the plurality of capacitor storage nodes comprises:

forming an insulative layer;

forming individual storage nodes received within the insulative layer;

forming protective caps over the capacitor storage nodes; and

selectively removing material of the insulative layer relative to the protective caps and partially exposing respective storage node portions; and

the etching of the common cell electrode layer comprises forming individual cell electrode bands around the node portions which were previously exposed and portions of the protective caps.

39. A method of forming capacitor-over-bit line memory circuitry comprising:

forming an opening in a first insulative material;

forming a conductive capacitor storage node within at least a portion of the opening;

forming a second insulative material over the capacitor storage node;

selectively removing portions of the first insulative material relative to the second insulative material and exposing a portion of the conductive capacitor storage node; and

forming a capacitor dielectric layer and a cell electrode layer operably proximate the exposed portion of the conductive capacitor storage node.

40. The method of claim 39, wherein:

the forming of the conductive capacitor storage node comprises partially filling the opening with conductive material; and

the forming of the second insulative material comprises filling a remaining opening portion with second insulative material.

41. The method of claim 39, wherein:

the forming of the conductive capacitor storage node comprises only partially filling the opening with conductive material; and

the forming of the second insulative material comprises filling a remaining opening portion with second insulative material.

42. The method of claim 39, wherein:

the forming of the conductive capacitor storage node comprises partially filling the opening with conductive material;

the forming of the second insulative material comprises filling a remaining opening portion with second insulative material; and

the removing of the portions of the first insulative material comprise exposing a side surface of the storage node.

43. The method of claim 39, wherein:

the removing of the portions of the first insulative material comprises exposing a side surface of the storage node; and

the forming of the cell electrode layer comprises forming a band of cell electrode layer material around the side surface which was previously exposed.

44. The method of claim 39, wherein:

the forming of the conductive capacitor storage node comprises partially filling the opening with conductive material;

the forming of the second insulative material comprises filling a remaining opening portion with second insulative material;

the removing of the portions of the first insulative material comprises exposing a side surface of the storage node; and

the forming of the cell electrode layer comprises forming a band of cell electrode layer material around the side surface which was previously exposed.

45. A method of forming capacitor-over-bit line memory circuitry comprising:

forming a plurality of openings in a first insulative material;

less than filling the openings with a conductive material comprising capacitor storage nodes;

filling the remaining openings with a second insulative material;

etching the first insulative material faster than any of the second insulative material sufficient to expose portions of individual capacitor storage nodes;

forming a capacitor dielectric layer and a common cell electrode layer operably proximate portions of the conductive capacitor storage nodes which were previously exposed;

anisotropically etching the common cell electrode layer and isolating individual cell electrodes over individual respective capacitor storage nodes; and

electrically interconnecting some of the isolated individual cell electrodes with conductive material.

46. The method of claim 45, wherein the less than filling of the openings comprises overfilling the openings with the conductive material and removing overfilled portions of the conductive material.

47. The method of claim 45, wherein the etching of the common cell electrode layer comprises forming respective bands around the individual storage node portions which were previously exposed.

48. The method of claim 45, wherein the interconnecting of the isolated cell electrodes comprises:

forming a third insulative material over the isolated cell electrodes;

etching a trench into the third insulative material and exposing the isolated individual cell electrodes; and

filling the trench with conductive material.

49. The method of claim 45, wherein:

the etching of the common cell electrode layer comprises forming respective bands around the individual storage node portions which were previously exposed; and

the interconnecting of the isolated cell electrodes comprises:

forming a third insulative material over the isolated cell electrodes;

etching a trench into the third insulative material and exposing some of the band portions of the individual storage node portions; and

filling the trench with conductive material.

50. A method of forming capacitor-over-bit line memory circuitry comprising:

forming an array of storage nodes arranged into columns;

first electrically interconnecting the array of storage nodes in a capacitor array configuration with a common cell electrode layer;

conducting a maskless etch within the array of the cell electrode layer to remove selected portions thereof sufficient to isolate cell electrodes over individual respective storage nodes; and

second electrically interconnecting some of the isolated cell electrodes with conductive material.

51. The method of claim 50, wherein the first electrically interconnecting of the array of storage nodes comprises forming the common cell electrode layer over and laterally proximate the storage nodes.

52. The method of claim 50, wherein the conducting of the maskless etch comprises anisotropically etching the cell electrode layer.

53. The method of claim 50, wherein the conducting of the maskless etch comprises forming a band of cell electrode layer material around portions of the respective storage nodes.

54. The method of claim 50, wherein the forming of the array of storage nodes comprises forming insulative caps over and not laterally proximate conductive material comprising the storage nodes.

55. The method of claim 50, wherein:

the forming of the array of storage nodes comprises forming insulative caps over and not laterally proximate conductive material comprising the storage nodes; and

the conducting of the maskless etch comprises forming a band of cell electrode layer material around portions of the respective storage nodes and portions of their associated insulative caps.

56. A method of forming a series of capacitors comprising forming a plurality of first and second capacitor electrode layers separated by intervening dielectric layers, one of the first and second capacitor electrode layers being formed, at least in part, by conducting a maskless anisotropic etch of conductive material comprising the one layer.

57. The method of claim 56, wherein the conducting of the anisotropic etch comprises forming a band comprising conductive material of the one layer around conductive material of the other layer.

58. The method of claim 56 further comprising forming a protective cap of material over the other of the layers prior to conducting the maskless anisotropic of the conductive material comprising the one layer.

59. The method of claim 56 further comprising forming a protective cap of material over the other of the layers prior to conducting the maskless anisotropic of the conductive material comprising the one layer, and wherein the conducting of the anisotropic etch comprises forming a band comprising conductive material of the one layer around conductive material of the other layer.

60. Integrated circuitry comprising:

a capacitor storage node having an uppermost surface and a side surface joined therewith;

a protective cap over the uppermost surface;

a capacitor dielectric layer over the side surface; and

a cell electrode band disposed proximate at least a portion of the storage node side surface and not over the storage node uppermost surface.

61. The integrated circuitry of claim 60, wherein the protective cap has a side surface, and the cell electrode band is disposed laterally proximate at least a portion of the protective cap side surface.

62. The integrated circuitry of claim 60, wherein the cell electrode band is disposed over less than an entirety of the storage node side surface.

63. The integrated circuitry of claim 60, wherein the cell electrode band has an uppermost portion which extends elevationally higher than any material of the capacitor storage node.

64. The integrated circuitry of claim 60, wherein:

the protective cap has a side surface, and the cell electrode band is disposed laterally proximate at least a portion of the protective cap side surface; and

the cell electrode band has an uppermost portion which extends elevationally higher than any material of the capacitor storage node.

65. The integrated circuitry of claim 60, wherein:

the cell electrode band is disposed over less than an entirety of the storage node side surface; and

the cell electrode band has an uppermost portion which extends elevationally higher than any material of the capacitor storage node.

66. Integrated circuitry comprising:

a capacitor storage node having an uppermost surface;

an insulative material overlying the uppermost surface;

a capacitor dielectric functioning region discrete from the overlying insulative material and disposed operably proximate at least a portion of the capacitor storage node; and

a cell electrode layer disposed laterally proximate the capacitor dielectric functioning region and the overlying insulative material.

67. The integrated circuitry of claim 66, wherein a substantial portion of the dielectric functioning region is disposed only laterally proximate the capacitor storage node.

68. The integrated circuitry of claim 66, wherein the dielectric functioning region comprises a layer of dielectric material which extends over the overlying insulative material and defines a non-dielectric functioning region.

69. The integrated circuitry of claim 66, wherein the dielectric functioning region defines a band of dielectric material which laterally encircles at least a portion of the storage node.

70. The integrated circuitry of claim 66, wherein the cell electrode layer defines a band of conductive material which laterally encircles at least a portion of the storage node.

71. The integrated circuitry of claim 66, wherein the cell electrode layer defines a band of conductive material which laterally encircles at least a portion of the storage node and comprises an uppermost band portion which extends elevationally higher than the storage node uppermost surface.

72. A capacitor-over-bit line memory array comprising:

a substrate;

a pair of spaced-apart conductive lines disposed over the substrate;

a pair of diffusion regions received within the substrate operably proximate the conductive lines;

conductive material disposed over and in electrical communication with the diffusion regions, the conductive material extending away from the diffusion regions;

a pair of capacitor storage nodes, each of which being operably joined with and in electrical communication with a respective one of the diffusion regions through the conductive material disposed thereover, each storage node having an uppermost surface and a side surface joined therewith;

a protective cap over each uppermost surface;

a capacitor dielectric layer over each side surface; and

a cell electrode band disposed proximate at least a portion of each storage node side surface and not over the associated storage node uppermost surface.

73. The capacitor-over-bit line memory array of claim 72, wherein each protective cap has a side surface, and the cell electrode band associated therewith is disposed laterally proximate at least a portion of the protective cap side surface.

74. The capacitor-over-bit line memory array of claim 72, wherein each cell electrode band is disposed over less than an entirety of its associated storage node side surface.

75. The capacitor-over-bit line memory array of claim 72, wherein each cell electrode band has an uppermost portion which extends elevationally higher than any material of its associated capacitor storage node.

76. The capacitor-over-bit line memory array of claim 72, wherein:

each protective cap has a side surface, and the cell electrode band associated therewith is disposed laterally proximate at least a portion of the protective cap side surface; and

each cell electrode band has an uppermost portion which extends elevationally higher than any material of its associated capacitor storage node.

77. The capacitor-over-bit line memory array of claim 72, wherein:

each cell electrode band is disposed over less than an entirety of its associated storage node side surface; and

each cell electrode band has an uppermost portion which extends elevationally higher than any material of its associated capacitor storage node.